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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/586,995	08/20/2008	Jussi-Pekka Tervaluoto	915-007.198	9068

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EXAMINER	
AKINYEMI, AJIBOLA A	
ART UNIT	PAPER NUMBER
2618	
MAIL DATE	DELIVERY MODE
01/05/2011	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/586,995	TERVALUOTO ET AL.	
	Examiner	Art Unit	
	AJIBOLA AKINYEMI	2618	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 September 2010*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 4-12* is/are rejected.

7)☒ Claim(s) *3* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 July 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 10/18/2010 has been entered.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. The factual inquiries set forth in Graham **v.** John Deere Co., 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. Claims 1, 4-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Admitted prior art henceforth "Admission" and further in view of Yamaji (Patent No.: US 6381449 B1) and Darabi (Patent No. US 6889037B2).

With respect to claim 1:

Admission discloses a mixer circuit comprising a down-conversion mixing component (fig.2, item 23) arranged for down-converting an input radio frequency signal (RF IN) and a load circuit connected to output terminals of said down-conversion mixing component (fig. 2, item 24). Admission does not explicitly disclose active load circuit and modulator arranged for modulating a flicker noise produced by said active mixer load away from the signal band of a signal output by said down-conversion mixing component. Yamaji (same field of endeavor) discloses active load (fig.2, item 23). It would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize the teachings of Yamaji into the teachings of Admission in order to obtain the desired receiving characteristic with few current consumption or reduce distortion. Darabi discloses a mixer circuit modulating a flicker noise (col.2, lines 26- col.3, lines 13). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize the teachings of Darabi into the teachings of Admission in view of Yamaji for the purpose of increase the receiver's voltage gain and to reduce or eliminate the flicker noise.

With respect to claim 4:

Admission discloses a Mixer circuit wherein said down-conversion mixing component (fig.2, item 23) is adapted to down-convert radio frequency current mode signals (parag.0016).

With respect to claim 5:

Admission discloses a Mixer circuit wherein said down-conversion mixing component (fig.2, item 23) is adapted to down-convert radio frequency voltage mode signals (fig.2, Urf+ and Urf- is being down-converted by item 23).

With respect to claim 6:

Admission discloses a receiver circuit for receiving radio frequency signals and for providing corresponding down-converted signals, which receiver circuit comprises a mixer circuit (fig.2, item 23) according to claim 1.

With respect to claim 7:

Admission discloses a receiver circuit wherein at least said mixing circuit (fig.1, item 12) and at least one component of said receiver circuit (fig.1, item 15) arranged for processing digital baseband signals are integrated in a single chip.

With respect to claim 8:

Admission discloses a chip comprising a mixer circuit (fig.2, item23) according to claim1

With respect to claim 9:

Admission discloses a chip wherein said mixer circuit is implemented on a said chip with a deep sub-micron semiconductor technology (parag.0014).

With respect to claim 10:

Admission discloses an apparatus comprising a mixer circuit (fig.2, item23) according to claim1.

With respect to claim 11:

Admission discloses a method for use in a mixer circuit comprising a down-conversion mixing component (fig.2, item 23) and a load circuit (fig.2, item 24) said method comprising: down-converting a received radio frequency signal by means of said down-conversion mixing component (fig.2, item 23); controlling an output voltage of said down-conversion mixing component by means of a load of said load circuit (fig.2, item 24). Admission does not explicitly disclose active load and modulating a flicker noise produced by said active mixer load away

from a signal band of said down-converted radio frequency signal. Yamaji (same field of endeavor) discloses active load (fig.2, item 23). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the above limitation in order to obtain the desired receiving characteristic with few current consumption or reduce distortion. Darabl discloses a mixer circuit modulating a flicker noise (col.2, lines 26- col.3, lines 13). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the above limitation in order to increase the receiver's voltage gain and to reduce or eliminate the flicker noise.

With respect to claim 12:

Admission discloses an apparatus comprising: means for down-converting an input radio frequency signal (fig.2, item 23); and load means (fig.2, item 24). Admission does not disclose means for providing active load and modulating means connected to output terminals of said means for down-converting for modulating a flicker noise produced by said active mixer load means away from a signal band of a signal output by said means for down-converting. Yamaji (same field of endeavor) discloses active load (fig.2, item 23). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the above limitation in order to obtain the desired receiving characteristic with few current consumption or reduce distortion. Darabl discloses a mixer circuit modulating a flicker noise (col.2, lines 26- col.3, lines 13). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the above limitation in order to increase the receiver's voltage gain and to reduce or eliminate the flicker noise.

Allowable Subject Matter

5. Claim 3 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

Applicant's arguments with respect to claim1, 3-12 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to AJIBOLA AKINYEMI whose telephone number is (571)270-1846. The examiner can normally be reached on monday- friday (8.30-5pm) Est.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, YUWEN PAN can be reached on (571) 272-7855. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/A. A./

Examiner, Art Unit 2618

/Duc Nguyen/

Supervisory Patent Examiner, Art Unit 2618